A High Performance RF Power Amplifier with Protection against Load Mismatches

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Abstract **— A high performance power amplifier is presented which includes a protection circuitry against load impedance variations. Load mismatches produce peak voltages on the power transistor collector that give rise to breakdown conditions and hence to permanent faults. The protection circuitry is based on a feedback loop that acts on the amplifier gain to limit the overdrive of the output transistor. A monolithic power amplifier for 1.8-GHz DCS-PCS applications was integrated in a silicon bipolar technology with a 4.3-V breakdown voltage. The amplifier delivers a 33-dBm output power with 51% power-added efficiency and 33-dB gain at a nominal 3-V supply voltage. Standing wave ratio was tested up to 20:1 for all phases with a supply voltage up to 3.8 V without damage to the device.**

I. Introduction

Low supply voltage and high efficiency are key issues in power amplifier (PA) design. To meet this target, GaAs-based PAs are commonly used. However, they are not cost-competitive devices as demanded for a high-volume production. It is well known that silicon-based technologies have an inherent advantage in implementing low-cost RFICs over III-V semiconductors. Consequently, efficient RF power amplifiers in pure silicon technology have been attracting increasing attention over the last few years [1]-[3].

The high performance that can be achieved with a bipolar technology [4] has to be traded for device ruggedness. This regards the ability of the device to tolerate load conditions that are different from the nominal ones. Standing wave ratio (SWR) is commonly used to define the percentage of load mismatch.

Typically, device testing procedures for commercial PAs may demand a SWR up to 20:1. With a power supply of 3 V, this target can only be achieved with a breakdown voltage (BV_{CEO}) higher than 15 V. However, a high breakdown voltage results in a low power-added efficiency (PAE). As reported in [4], by increasing BV_{CEO} from 3.4 V to 6.4 V the efficiency of the transistor decreases from 83% to 69%.

Protection circuitries can be adopted instead of technological solutions. An example is proposed in [5]. It uses a clamping circuit that limits the maximum peak voltage at the collector of the output transistor.

In this paper a three-stage power amplifier is proposed which includes a protection circuitry to overcome the detrimental effects of load impedance mismatches. By using a very low cost bipolar process with a BV_{CEO} of 4.3 V, a monolithic power amplifier for 1.8-GHz DCS-PCS wireless communications was designed which is able to tolerate a SWR as high as 20:1 with a supply voltage up to 3.8 V. The amplifier delivers 33-dBm output power with 51% PAE and 33-dB gain at a 3-V power supply. A reference power amplifier without protection was also integrated for performance comparison. The latter is analyzed in section II. The protection technique is presented in Section III. Finally, the measured performance is detailed in Section IV.

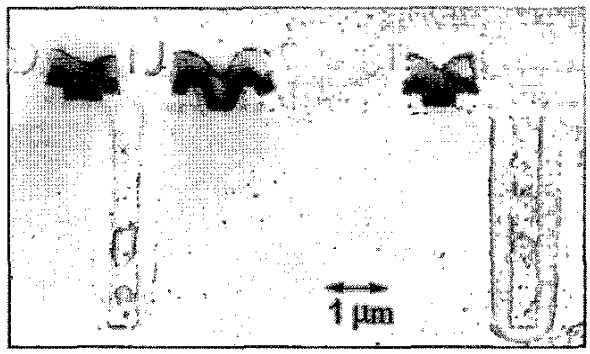

Fig. 1. HSB3 process TEM cross section.

II. Technology And Reference Power Amplifier

A. Silicon Bipolar Technology

The devices were fabricated in a 46-GHz-f_T double-poly 0.8-μm self-aligned-emitter silicon bipolar process (HSB3) by STMicroelectronics. This is a low-cost technology, which requires only 17 mask steps. It allows oxide trench isolation, three metal layers, poly resistors, and metal-insulator-metal (MIM) capacitors with 0.7 fF/μm^2. On-chip spiral inductors are also available (3-μm-thick

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AlSiCu third metal layer) with Q values up to 10 at 2 GHz and resonant frequencies above 15 GHz. Fig. 1 shows a TEM cross section of a transistor with a 0.8-μm emitter mask size.

The standard process has a BV_{CEO} of 3.3 V. The PAE-BV_{CEO} trade-off for a 20-dBm power transistor is shown in Fig. 2. A technology version with 4.3-V BV_{CEO} was used for the PA design, which appeared to be a good compromise between PAE and robustness at a nominal 3-V power supply.

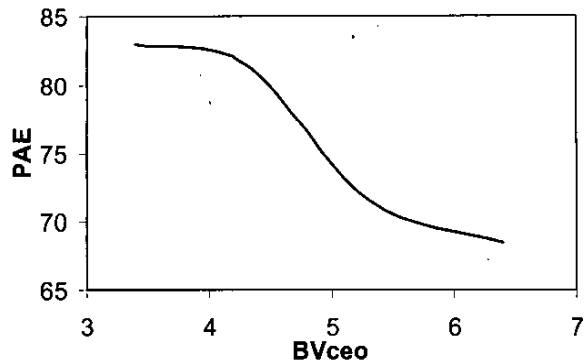

Fig. 2. PAE versus breakdown voltage.

B. Reference Power Amplifier

Fig. 3 shows a simplified schematic of the reference three-stage power amplifier. The first stage is a variable-gain amplifier (VGA), which is operated at maximum gain under nominal conditions as explained in Section III.

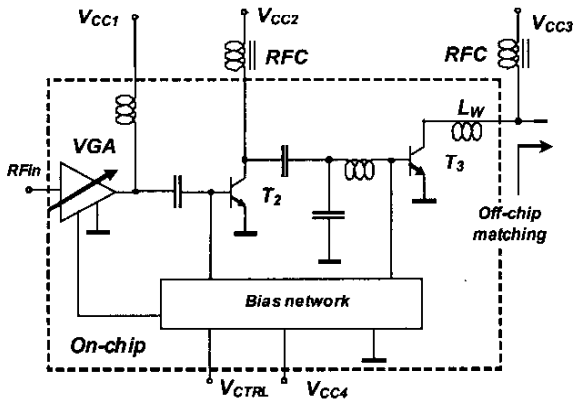

Fig. 3. Simplified schematic of the reference PA.

In DCS-PCS systems, linearity is not a critical aspect and high-efficiency operation classes can be used. As shown in Fig. 4, a series-resonant load [4] was adopted to provide a high reactive impedance for the harmonics of the fundamental frequency. A pulsed collector voltage and a sinusoidal current are achieved (mixed-C mode [6] or Class C-E [7]).

The on-chip inter-stage matching networks were designed for maximum gain under large-signal conditions. A bond-wire inductance and capacitor were used between the first and second stages, whereas two capacitors and a spiral inductor were employed between the second and third stages. On-chip input matching network was also implemented by means of two bond-wire inductances at the emitter and base of the first stage.

A bias circuit was included allowing power control by varying the base quiescent current of each stage through the external voltage V_{CTRL}.

The die was molded in a 24-pin 5×5-mm LPCC package, which provides an exposed bottom pad for RF grounding and heat dissipation. To minimize emitter inductance, a large number of staggered down-bonding wires were used to connect the die emitter ground planes and the exposed pad.

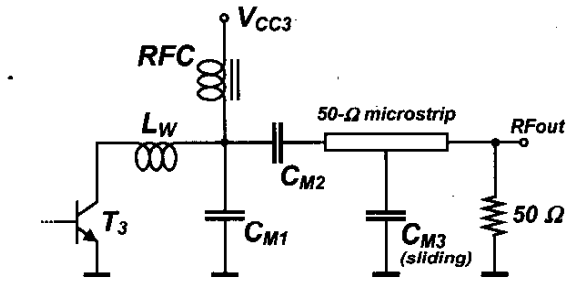

Fig. 4. Output matching network.

III. The Protection Technique

High-efficiency operation classes require the PA to be overdriven to achieve optimum voltage and current waveforms at the collector of the output transistor. The simulated curves are shown in Fig. 5 for a 3-V supply voltage. It is apparent that the maximum voltage is three times higher than the supply voltage. Under load mismatch conditions, peak voltages even five times higher than the supply voltage can occur, hence pushing the output transistor into the breakdown region. Such an effect can be avoided by including an additional control loop that detects the collector peak voltage and reduces the overdrive by limiting the overall amplifier gain. Then the output transistor is taken out of the high-efficiency operation mode and conducted to a safe operating region.

The block diagram of the PA control loop is shown in Fig. 6. A high-input-impedance sensing network scales

down the collector voltage with a negligible loading effect on the power transistor. In this way, the nominal performance is preserved. The scaled-down signal is applied to an envelope detector delivering an output signal proportional to the collector peak voltage. The rectified waveform is compared with a reference voltage and the difference between the two signals is amplified by the error amplifier. The error signal drives the control terminal of the VGA, which is also externally available for testing purposes (V_{TEST}). It is worth mentioning that the gain control does not affect the input impedance since the quiescent current in the input transistor T1 remains constant. Therefore, input matching is preserved.

A detailed schematic of the control loop is shown in Fig. 7. A high-speed loop must be guaranteed to track collector voltage variations. Moreover, the sensing network and the envelope detector require proper design to avoid local instability due to negative impedance at the common-collector input. Finally, frequency stability must be provided. To this purpose, a 15-pF dominant-pole compensation capacitance (Cc) was included.

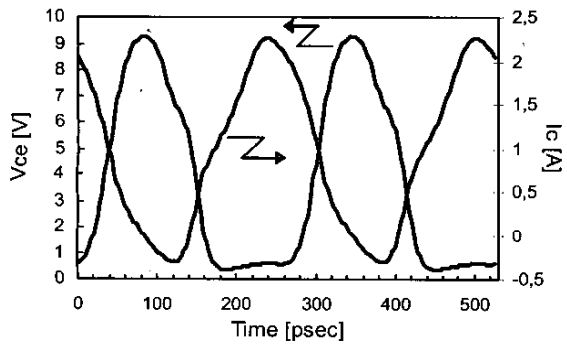

Fig. 5. Simulated collector voltage and current (3-V supply voltage).

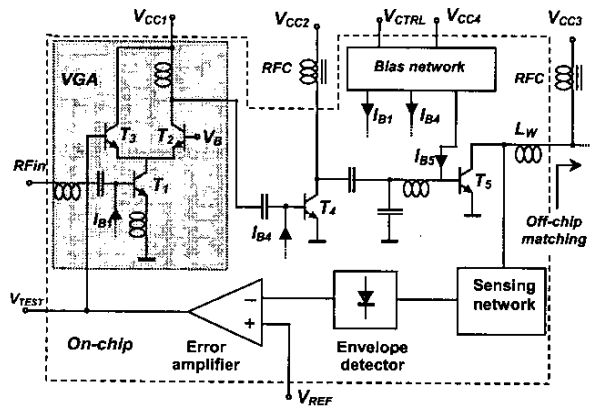

Fig. 6. A simplified schematic of the protected PA.

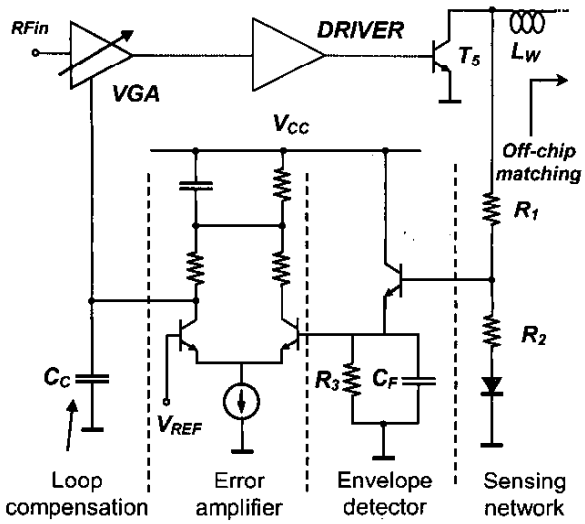

Fig. 7. Schematic of the control loop.

IV. Measurement Results

The die photo of the integrated PA is shown in Fig. 8 where the blocks of the control loop are highlighted. The additional control circuitry leads to a very small increase in the overall silicon area, which is 1.9 mm × 1.9 mm.

Measurements were carried out using the same set-up and output matching network for the PA both with and without protection. The two devices were soldered on a 400-μm-thick FR4 printed-circuit board (PCB). They exhibited identical performance in terms of output power, gain and PAE under nominal bias and load conditions.

The output power and PAE versus input power at 1.8 GHz and 3-V power supply are shown in Fig. 9. A PAE of 51% was achieved at 33-dBm output power and 33-dB gain. Output SWR tests were carried out on a large number of samples. The PA without protection was damaged by a SWR lower than 8:1 at a 3.3-V supply voltage. On the contrary, the PA with protection revealed no damage with SWRs as high as 20:1 and supply voltages up to 3.8 V for all phases.

Monitoring of the collector peak voltage V_{PK} was also possible according to the following equation.

$$V_{PK} = k \cdot V_{REF} + V_{BE} \qquad (1)$$

where V_{REF} is the external reference voltage and k is the scale factor of the sensing circuit.

Thanks to (1), by varying V_{REF} and looking at the error amplifier output V_{TEST}, a nominal collector peak voltage of 9.5 V was estimated with the PA delivering a 33-dBm output power under a 3-V supply voltage. This peak value corresponds to the operation class selected. Moreover, the

collector peak voltage for a SWR of 10:1 at a supply voltage of 2.3 V was measured as a function of the phase angle, using the same approach. Comparison with simulated peak voltage is shown in Fig. 10, which reveals an excellent agreement. The high peak values (greater than four times the power supply) demonstrate that the loop bandwidth and the sensing network were correctly designed to follow fast variations of the collector voltage.

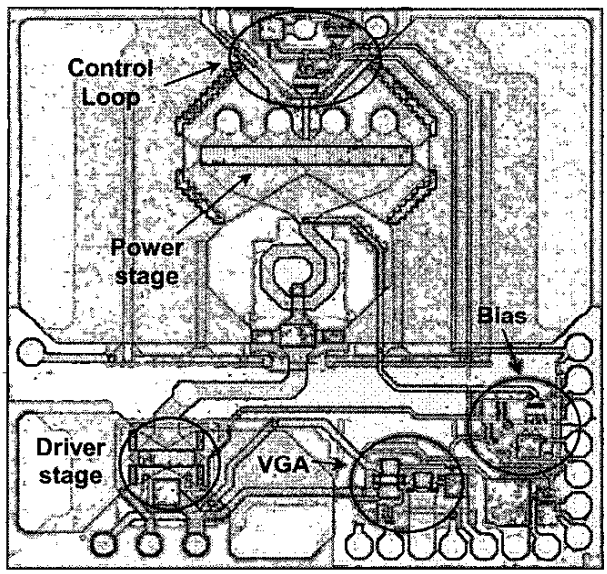

Fig. 8. Die photo of the protected PA.

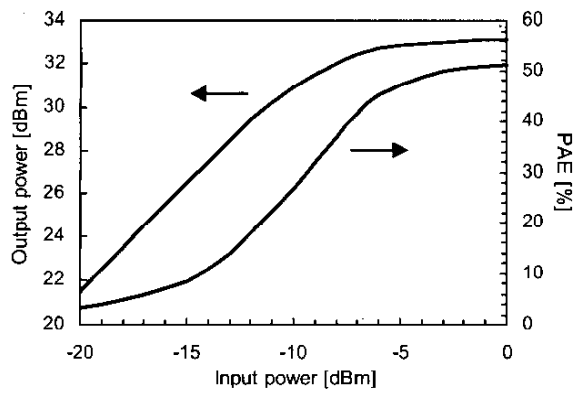

Fig. 9. Output power and PAE versus input power.

V. Conclusions

A high performance RF PA for DCS-PCS applications protected against faults coming from load mismatches has been presented. The circuit was implemented in a silicon bipolar technology with 4.3-V BV_{CEO}. An output power and a PAE of 33 dBm and 51%, respectively, were achieved under a 3-V power supply. Ruggedness was validated by 20:1 SWR testing under any phase condition and with a supply voltage up to 3.8 V.

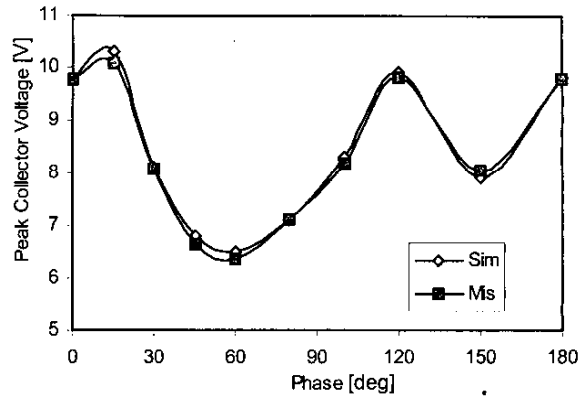

Fig. 10. Comparison between simulated and measured peak collector voltage.

Acknowledgment

The authors wish to thank Giovanni Conti, STMicroelectronics, Catania, Italy, for assistance with measurements.

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